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EFFECT OF REDUCTION IN GATE OXIDE THICKNESS WITH DIFFERENT MATERIALS FOR 100NM MOSFET

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Abstract – In recent years, the growth of IC industry has been driven by scaling of metal-oxide-semiconductor field effect transistor (MOSFET). The device has been used as a fast switch in compute intensive applications. The switching speed of a MOSFET is highly dependent on the choice of gate oxide material and its thickness. In this paper, we present a comparative analysis of the effect of scaling of gate oxide thickness on the performance of 100nm n-type MOSFET for different gate oxide materials.

Keywords — MOSFET, Gate oxide, Switching speed, Threshold voltage, Dielectric constant

I. INTRODUCTION

Metal-oxide-semiconductor field effect transistor (MOSFET) is the workhorse for contemporary digital design. This device can be used as switch in many applications and offers little parasitic effects [1]. Digital computers use transistors as a basic mechanism for storing and moving data. The device can be produced at a very large scale due to its large integration density and simple and standard fabrication process [2]. The drift of scaling was predicted by Moore's law, according to which the transistor count on an integrated circuit doubles every 18 months. Alternative gate materials with dielectric constant higher than than of SiO_2 help to keep up with the trends of Moore's law [3, 4].The layers of these high – k materials can be grown thick to reduce the direct tunneling current through gate.

II. MOSFET: DEVICE OPERATION AND STRUCTURE

We used the simplest two dimensional three terminal device model for n-type MOSFET as shown below in Fig. 1. It is called an NMOS transistor because the major charge carriers that form current are negatively charged electrons. The fourth terminal called body is not considered due to its secondary function in the MOSFET operation.
Positive voltage is applied to gate terminal to create the channel between drain and source region. The performance of high speed logic circuits depend on source-drain saturation current called drive current. The source-drain saturation current for an n-type MOSFET can be written as the following equation [5, 6]

$$I_d = \frac{\beta_n (V_{gs}-V_t)^2}{2} \quad (1)$$

where β_n is conduction parameter of MOSFET and is inversely dependent on gate oxide thickness, d. Hence, mathematically, it can be deduced that

$$I_d \propto \frac{1}{d} \quad (2)$$

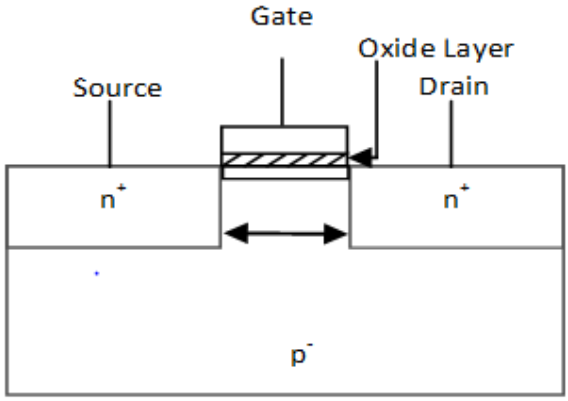

Fig. 1 2-dimensional structure of n-type MOSFET [5, 7]

Decreasing the oxide layer thickness produces high gate capacitance, which leads to more drive current, I_d for same gate voltage, V_g [8, 9]. Taking the gate oxide as the parallel plate capacitor, the gate capacitance is defined as the following equation [5, 6]

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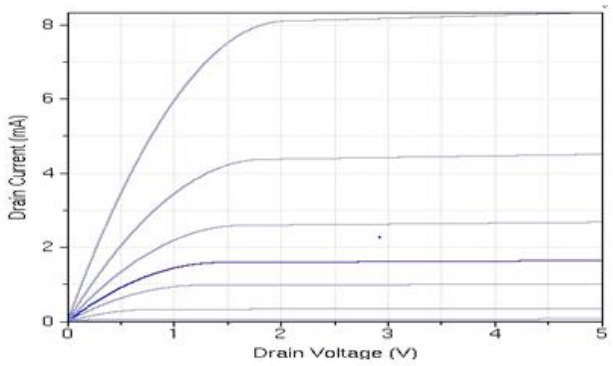

Fig. 2 I_d v/s V_{ds} characteristics of n-type MOSFET

$$C_{ox} = \frac{k\varepsilon_0}{d}A \quad (3)$$

where, k is the dielectric constant for gate oxide material, ε_0 is the permittivity of free space, and A is the gate area. Once the applied gate voltage is above threshold voltage, V_T channel is formed between source and drain diffusion region. As we increase the drain voltage, an increase in drain current is observed.

III. GATE DIELECTRIC MATERIALS

The fabrication of MOSFET device is a sequence of steps i. e. photo lithographical exposure and etching, material deposition etc, which are executed repeatedly. Each of these steps also consist a number of basic steps. High – k gate dielectrics can be easily deposited by atomic layer deposition (ALD) [10]. The dielectric constant of a material depends on the deposition method, composition and microstructure of the material. Generally, a high-k oxide material should satisfy the following properties:

1) *High dielectric constant:* Initially, due to high production cost of alternative gate oxide material, the dielectric constant of material should be sufficiently large to support the performance improvements of IC industry [11, 12].

2) *Band gap and barrier height*: To reduce gate leakage current, sufficient band gap of gate oxide material is required [13]. Also the barrier height of gate oxide material is important as it affects the gate tunnelling current [14].

3) *Thermodynamically stability*: At high temperature, the amorphous gate oxide material may change into crystals. The material in this form may lead to additional conduction path for leakage current through gate [15]. It may result into formation of low – k oxide interface

4) *Interface quality*: The possibility of formation of silicates at high – k gate material and Silicon should be avoided, as it may create additional conduction path for gate leakage current [16].

5) *Process compatibility*: The high k – gate material must be compatible with current CMOS fabrication process flow and other materials used in CMOS integrated circuits.

6) *Fixed oxide charge*: The oxide-substrate interface must have minimum oxide fixed charges and interface trap charges to minimize carrier scattering at the underlying channel [10, 17]. The presence of these charges in at the interface reduces the mobility of charge carrier in channel.

7) Good reliability and long life time: Reliability of high – k gate structures may be influenced by the interfacial layer as well as high – k oxide layer. Due to charge trapping at oxide interface, serious reliability issues occur due to instabilities in threshold voltage, V_T. There is a clear linkage between performance and reliability issues of a MOSFET device [18].

A variety of dielectric materials has been developed for gate oxide. Here, we have considered only four popular materials, which are listed in Table 1.

A. SiO_2

The most common amorphous oxide material used for MOSFET gate is SiO_2. This material offers following interesting properties of:

1) Large band gap i.e. ~ 9eV.
2) Good thermodynamic stability on Silicon surface
3) Easy to grow thermally on Silicon surface with high quality.

Table 1 Different Oxide Materials with Their Dielectric Constant and Crystal Structures [19]

S. No.	Material	Dielectric constant (k)	Crystal Structures
1	SiO_2	3.9	Amorphous
2	Al_2O_3	9	Amorphous
3	$HfSiO_4$	11	Monoclinic tetragonal cubic
4	HfO_2	25	Monoclinic tetragonal cubic

B. Al_2O_3

This material has the appealing property of large band gap, good stability, amorphous and robust on Silicon against formation of SiO_2 [12] . However, it can be used for short term at gate electrode due to its low value of k_{ox} which lies between 8 and 10, which limits its capability to increase drive current in MOSFETs. Also significant mobility degradation has been observed in this case.

C. HfO_2 and $HfSiO_4$

Usually, the high – k materials have small band gap which leads to more gate leakage current. But HfO_2 can be effectively used to replace SiO_2 due to its large band gap. These two materials are members of Pseudobinary alloy

family $(HfO_2)_x(SiO_2)_{1-x}$. Hafnium oxide (HfO_2) is a colorless inorganic compound with a band gap of 5.3~5.7 eV and commonly known as hafnia [3, 20]. The crystal structure of such dielectrics is monoclinic tetragonal cubic. The material is quite inert with its high - k value of 25 as shown in Table 1. Due to high value of band gap, E_g leakage current decreases in layers of such materials. Amorphous HfO_2 is deposited to form the gate oxide layer in modern semiconductor technology. The layers of these materials are stable on Si upto high temperatures [21, 22]. The material $HfSiO_4$ is formed by alloying hafnium oxide with silicon known as hafnium silicate. It gives the advantage of increased crystallization temperature and melting point of hafnium oxide.

IV. EXPERIMENTAL SET-UP

The simulation tool *MOSFETsim* was used, which displays drain current as a function of source-drain voltage for different values of gate voltage, gate dimensions, substrate material and oxide material in an n-type MOSFET [23]. The values of critical parameters like channel length, L_n = 100 nm, gate voltage V_g = 3V were taken for n-MOS device on p-type substrate with $n_i = 1.5 \times 10^{16}$ and k_{sub} = 11.9.

V. RESULTS AND DISCUSSION

As we decrease the oxide thickness, the gate voltage becomes more effective to invert the underlying channel region, which results in an ease of channel formation. Also the type of gate oxide material plays an important role. In case of SiO_2 as the dielectric material, it is observed that for gate voltage, V_g = 3V, the channel was not formed for oxide layer thickness above 50 nm. It is due to insufficient channel formed under gate due to large oxide thickness. The drain current starts to flow after thickness of gate oxide layer reduces to 50 nm and less as shown below in Table 2.

Table 2. Drain Current I_d with Different Gate Dielectric Materials

S. No.	Gate oxide thickness, d (nm)	Drain current, I_d (mA) for different Gate dielectric materials			
		I_d with SiO_2	I_d with Al_2O_3	I_d with $HfSiO_4$	I_d with HfO_2
1	100	0	0.2171	0.5554	4.0969
2	90	0	0.3791	0.8056	4.8779
3	80	0	0.6163	1.1476	5.867
4	70	0	0.9446	1.6191	7.1526
5	60	0	1.4443	2.2871	8.8824
6	50	0.0659	2.2003	3.2686	11.3271
7	40	0.3359	3.4062	4.801	15.0192
8	30	0.9938	5.5093	7.4276	21.2103
9	25	1.6157	7.236	9.5643	26.1771
10	20	2.6297	9.8572	12.7998	33.6547
11	15	4.4268	14.2784	18.2376	46.109
12	10	8.1819	23.1929	29.1653	71.0329

It is also analyzed that for other oxide materials like Al_2O_3, $HfSiO_4$ and Hafnium, the drain current starts to flows for oxide layer thickness even at 100nm. In general, it is observed from the Fig. 3, as we scale down the gate oxide thickness, more current flows in channel region. For the high - k material like HfO_2 we observed that for same gate voltage, V_g, more drain current is flowing. It is due to high permittivity, ε_{ox} offered by the materials like Al_2O_3, $HfSiO_4$ and HfO_2. Among the four oxide materials i. e. SiO_2, Al_2O_3, $HfSiO_4$ and HfO_2, the last one produces the maximum current for same gate voltage as shown below in Fig 3.

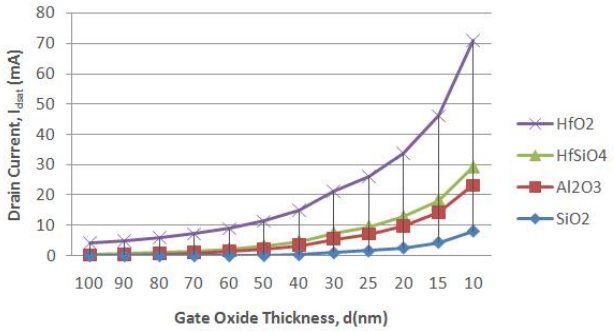

Fig. 3 Change observed in drain current I_d, w.r.t. reduction in gate oxide thickness for different gate oxide materials.

But, as HfO_2 may not be the best choice in the applications, which requires high crystallization temperature. In such cases, hafnium doped with silicon i.e. hafnium silicate like $HfSiO_4$ may be a better choice.

VI. CONCLUSION

The choice of gate dielectric material plays a key role in channel inversion. The use of high k-materials like hafnium/hafnium silicates results into more drain current for same oxide thickness.

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